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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,708	03/15/2004	Meng-Jyh Lin	LINM3016/EM	8974

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,708	LIN, MENG-JYH	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/23/05 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 3 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the phrase "wherein a resistance ratio of the resistor pair, a resistance of the reference resistor and an area ratio of the at least one transistor pair are adjusted to reduce temperature coefficient impact" on the last 2 lines of the claim is indefinite because it is not clear "temperature coefficient" of which element, or the "impact" of which element. Further, the above recitation appears to be misdescriptive since it is inconsistent with the disclosure since the specification does not recited adjusting a resistance ratio of the resistor pair (i.e., the resistor pair are not adjusted) since the specification (line 19 of page 5 to line 5 of page 6) recites "adjusting resistance ratio for the reference resistor 42 to resistor pair 411, 412" (i.e., it

is only adjusting the value of reference resistor). Clarification and/or appropriate correction is requested.

Claims 3 and 7 are indefinite because they include the indefiniteness of claim 1.

With respect to claim 3, the recitation "a detection voltage level of VBG*(R2 + R3)/R3" on line 2 is indefinite because the detection voltage level of VBG*(R2 + R3)/R3 is only true for the circuits in Figures 1 and 2 (applicant's admitted prior art), and the above equation/formula is not true for the circuit in Figures 4-7 since there is a voltage drop across transistor (Q2, Figures 4 and 6) and cascode transistors Q2A-Q2E (Figures 4 and 7). Thus, it is not clear how the voltage detection level of applicant's invention (Figures 4-7) is VBG*(R2 + R3)/R3. Clarification and/or appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Tasdighi (USP 5,814,995).

Note that Figure 7 of the Tasdighi reference discloses a voltage detector circuit (R1-R3, 65, 66, 56), which includes a resistor pair (R2, R3) connected to an input voltage (voltage at the connection junction of resistors R2 and R3); a reference resistor (R1) connected to one resistor (R2) of the resistor pair (R2, R3) for producing a comparison voltage (connection junction of R2 and R1); at least one transistor pair (65, 66) connected to the other resistor (R3) of the resistor pair (R2, R3) and the reference resistor (R1) for producing a reference detection voltage (connection junction of R3 and transistor 66); and a comparator (56) for comparing the first comparison voltage and the reference detection voltage for outputting a voltage level (Vout),

wherein the at least one transistor pair (65, 66) includes M cascode transistor pairs (M = 1 pair so it meets the limitation it is required M is a positive integer greater than 0). Note that the function recitation "wherein a resistance ratio of the resistor pair, a resistance of the reference resistor and an area ratio of the at least one transistor pair are adjusted to reduce temperature coefficient impact" on the last 2 lines of the claim is fully met because the structure of the detector circuit (R1-R3, 65m 66 and 56) in Figure 7 of Tasdighi is substantially the same as applicant's invention (Figure 4), see In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977), and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). Also, insofar as understood in claim 3, because the structure of the voltage detector circuit (R1-R3, 65m 66 and 56) in Figure 7 of Tasdighi is substantially the same as applicant's invention (Figure 4), so the comparator (56) also capable of detects the input voltage to be a detection voltage level of VGB*(R2 + R1)/R1 as applicant's invention, wherein VBG = the reference detection voltage, R2 is the resistance of the one resistor pair (R1, R2), and R1 is the reference resistor.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi (USP 5,814,995) in view of Malhi (USP 5,731,686).

With respect to claim 7, the voltage detector (R1-R3, 65, 66 and 56) in Figure 7 of Tasdighi as discussed above in claims 1 and 3 meets all the limitations of this claim except that

the voltage detector circuit further includes the switch coupled between the resistor pair and the input voltage. However, the Malhi reference discloses in Figure 3 a circuit that including a switch (216) connected between reference node 214 and the input signal for switching the circuitry between the standby state and operation state. Thus, it would have been obvious to one having skill in the art at the time the invention was made to modify the voltage detector circuit (R1-R3, 65, 66 and 56) in Figure 7 of Tasdighi by providing a switch connected between the resistor pair and the input voltage as taught by the Malhi reference for the purpose controlling operational state and standby state of the voltage detector circuitry and thus for saving the power consumption of the circuit because during a standby state, the switch would be off and thus no current can flow through the resistor pair. Thus, this modification/combination meets all the limitations of claim 7.

Response to Arguments

7. Applicant's arguments filed 11/23/05 have been fully considered but they are not persuasive.

Applicant argues that the transistor pair (R2, R3) in Figure 7 of Tasdighi is not connected to the input voltage (Vin), but connected to a resistor divider formed of RD and RU, so neither of resistors R2 and R3 of Tasdighi is used to partition the input voltage. However, this argument is not persuasive because the input voltage, as discussed in the rejection, is the voltage at the connection junction resistors R2 and R3 (i.e., the output of voltage divider RD-RU), and thus the resistor R2 is partition the input voltage (the voltage at the connection junction resistors R2 and R3).

With respect to the rejection under 35 U.S.C 103, in response to applicant's arguments against the reference (Malhi) individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:20am to 6:50pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 26, 2006

LONG NGUYEN
PRIMARY EXAMINER